MAINTAINING ELECTROMAGNETIC COMPATIBILITY THROUGH DESIGN FOR FABRICATION AND ASSEMBLY OF PRINTED CIRCUIT BOARDS (PCBs)

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ABSTRACT

Recent regulations have demanded that electronics manufacturing companies control emissions from their products and the susceptibility of their products to emissions from other products. In addition, unexpected product failure and the ever-present demands of technology are also forcing the electronics industry to face the need to maintain electrical integrity.

Our investigations into high-speed design techniques have shown three major causes of failure: emissions from interconnecting conductors; poor PCB layout and lack of technical knowledge in electromagnetic compatibility (EMC). Catching these kinds of electrical integrity problems early in the design phase allows designers to take timely action without jeopardising project time scales. The work reported here presents design for manufacturing guidelines and rules to maintain electrical integrity in printed circuit boards (PCBs). Currently, a common method for handling EMC is through compliance testing of the final product. Similarly, noise budget is measured on finished prototypes. Since product life cycles are reducing, dealing with EMC late in the design cycle is undesirable. The cost of fixing may also be higher at a final stage because only a few options are available to correct the problem. A 'find and fix' approach is no longer acceptable anymore.

More and more companies are facing or will soon be facing EMC and electrical integrity issues. The majority of analysis tools available today are targeted toward simulation engineers. Such tools are not easy to use and are dependent on the availability and accuracy of complex simulation models. Moreover, they also tend to be ineffective on how to correct potential EMC problems.

KEYWORDS: Design for Manufacture, EMC, PCB Design

1 INTRODUCTION

The electronics industry is ever-changing, a good indication of these changes is to consider microprocessor performance over the last few years. The graph shown in Figure 1 illustrates the past, present and future trends in microprocessor clock frequency thus necessitating the need for signal integrity issues so as to prevent or minimise the effects of electro-magnetic interference.

Interconnecting traces exhibit "parasitics" such as self inductance, self capacitance, mutual inductance and capacitance with their surroundings. These parasitics are very small factors with signals running at low frequencies, but cannot be ignored at high speed. Presently, the continual increase of clock frequencies and faster rise and fall times, cause interconnects to start act active as active elements of the design and interconnect delays start to become even greater then component delays. In other words, at higher frequencies, a signal trace becomes an interconnect component. A PCB trace alone can be represented as a transmission line consisting of series inductance and shunt capacitance elements distributed along the line.

At high speed, a signal propagating down the line has to charge up each inductor and capacitor element before it is passed to the next element. It is intuitively easy to understand that this charging process has the effect of reducing the propagation time and increase the impedance of the trace.

The characteristic impedance (electromagnetic wave resistance) of a PCB trace is determined primarily by its width, the PCB material and the thickness between signal layer and power plane. The physical construction of the PCB may be considered as a wave-guide made up of trace geometry, dielectric insulator and planes. A typical PCB layer cross-section can be can be divided in five different configurations: microstrip; embedded microstrip; dual microstrip; stripline and dual stripline. Each configuration has its own characteristic impedance and propagation delay.

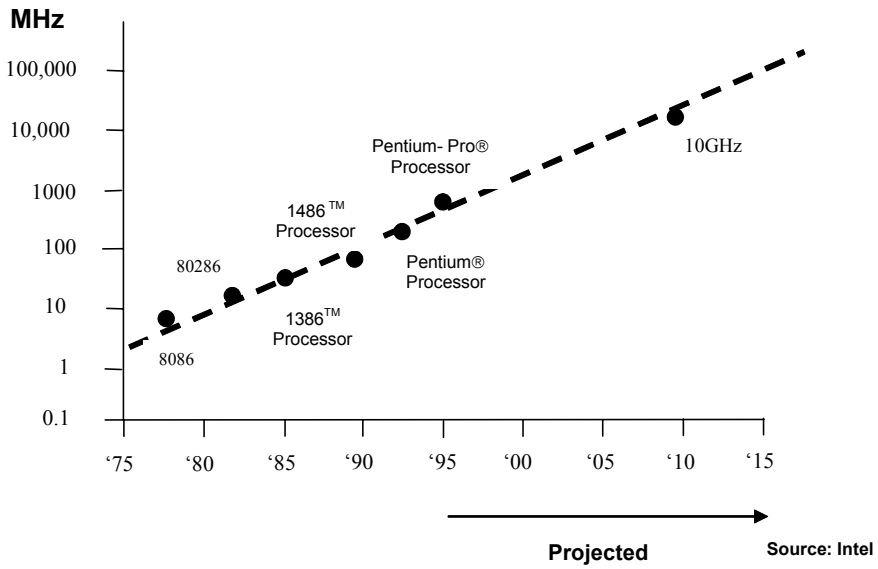

Figure 1:Moore's Law, Frequency with respect to time

Impedance is expressed as: $Z = \sqrt{\frac{L}{C}}$ ---------- (1)

L being the per unit length inductance and *C* the per unit length capacitance.

2 CROSS-SECTIONS OF VARIOUS TRANSMISSION LINE CONFIGURATIONS

Microstrip : *A track routed over a solid ground plane.*
Embedded Microstrip: *Same as microstrip but trace is buried in the insulator.*
Dual microstrip: *Two surface traces buried in the insulator.*
Stripline: *Case of a wire sandwiched between two planes.*
Dual stripline: *Two traces centred between two planes.*

With reference to figure 2, a signal runs faster on microstrip configuration than on stripline. So for a given delay, longer tracks are permitted with a microstrip configuration. It is important to note that, a wire routed in microstrip is not shielded from emissions by the power and ground planes as it would be the case of a wire routed in stripline.

Shielding in case of stripline gives typically a reduction of emissions by up to 10bB. For high speed boards, place power and ground planes directly adjacent. This will maximise the capacitive coupling and thus reduce supply noise. Also use extra ground planes (and not pwer planes) to isolate routing layers. For example, for an 8 layer PCB (4 routing), the best assignment for EMC performance is S1, G, S2, G, P, S3, G, S4 where S = signal routing layer, G = ground plane and P = power plane.

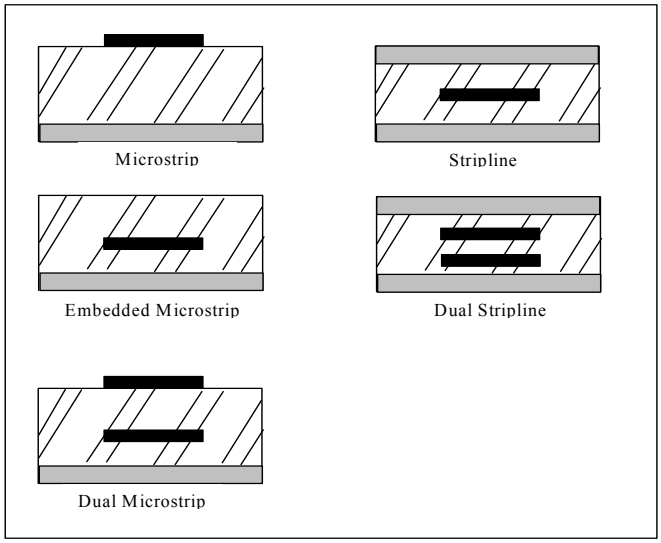

Figure 2: Cross-sections of various transmission line configurations

3 PROPAGATION DELAY

Propagation Delay is a complex function of many parameters including incluing inpedance and loading. Intended functionality requires that timing constraints have to be defined. Here are two examples. Delay control, see figure 3, if T_{pd} is too long, then the pulse will arrive too late for the intended function.

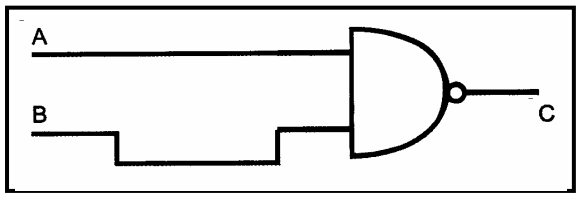

Figure 3: Delay control

Skew management, see figure 4, the path delay of A+C OR B+C must be equal to D within device tolerance. Important factors for skew management are gate propagation delays and copper trace delays. Effective skew management is ideally performed in the time domain not in the geometrical domain.

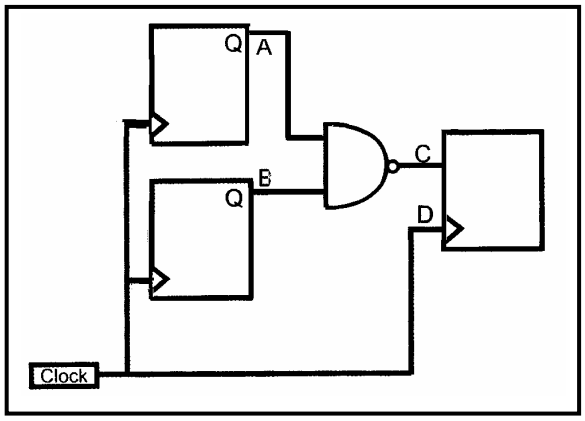

Figure 4: Skew management

4 ATTENUATION

At high frequencies, current density no longer becomes evenly distributed in the cross-section of the trace. The current density becomes higher near the surface of the trace and the resistor of the conductor increases. This skin effect has a consequence on the high harmonic frequencies and is responsible for signal degradation and attenuation. Because of the skin effect, a square pulse shape will become slightly rounded. Also, while the resistance increases with the frequency, the intrinsic trace inductance reduces and it is then the loop inductance that becomes the dominant paramater in thecharacteristic impedance. This inductance is a function of the geometry of the signal and its ground return path. In order to minimise these effects with high speed signals, short and wide tracks are highly recommended.

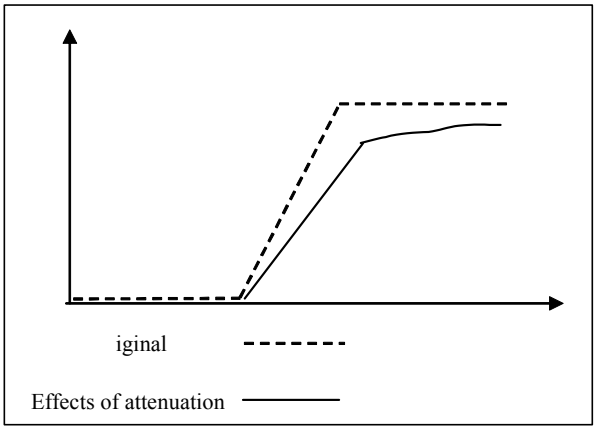

Figure 5: Effects Attenuation on an original pulse

5 REFLECTIONS

A signal propagating down a lossless line of constant characteristic impedance will travel along the line without distortion. However, when the signal arrives at the end of the line (after Td time), reflection will occur if the load impedance does not match the impedance of the conductor, see figure 6. The reflected wave travels back down the line and after Td time, it hits the source and is reflected back again but now from the source.

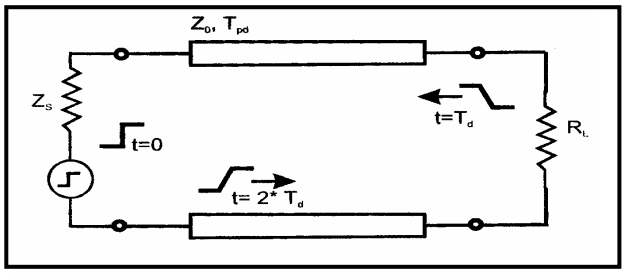

Figure 6: Chronlogy of a reflection

The signal is partially reflected, the amount of reflection is dependent on the magnitude of the impedance mismatch. The reflection coefficient, expressed as a percentage can be calculated as:

$$Kref = 100 \times \frac{(Zs - Z0)}{(Zs + Z0)} \quad \text{---------- (2)}$$

When the rise time of the signal is greater than the propagation delay down the trace, the reflections are masked by the slow rise of the signal. If the two-way propagation delay (source-end-source) is longer than the rise or fall times, then the reflection from the far end arrived after the initial transition is finished. The length beyond which the line should be terminated is given by:

$$L = \frac{Tr}{2 \times Td} \quad \text{---------- (3)}$$

Where: L = length of trace, Tr = edge rate, Td = loaded propagation delay.

Long nets may be subject to high amounts of reflection. For example, rise times of 2 nano-seconds require special consideration when the trace length is greater then 14 cm (for the stripline topology, FR-4 material). This length threshold is often called the critical length, it is the maximum permissible unterminated trace length. Different logic families with characteristic rise times will demand critical length of traces in order to reduce the impedance. Ensuring that traces are kept under their critical length is often unpractical. In such cases a termination scheme may be the best solution.

6 TERMINATION STRATEGIES

As mentioned earlier, in order to reduce reflections, the input impedance of the receiver must appear to match the impedance of the inductor. The reflection coefficient, expressed in percentage is calculated from equation (2). An input impedance of the receiver, larger than the conductor's impedance will cause over/undershoot, while the opposite will cause a drop in the pulse. The side affects of termination area: additional of extra delay to the signal; extra power consumption due to current requirement; and extra cost of component. Typically, such termination methods are recommended by the semiconductor vendor. Methods of termination comprise the following: series resistor; parallel resistor; Thevenin (split resistor); RC termination and diode clamp. With the exception of the diode clamp strategy, all other termination methods involve the output resistance of the driver that is non-linear and varies for most semiconductor processes over a wide range.

7 TOPOLOGY

Timing constraints are taken into account when selecting the appropriate net topology to control the arrival time of the signals at their respective receivers. Various topologies are used to achieve different objectives, figure 7 illustrates commonly used net topologies.

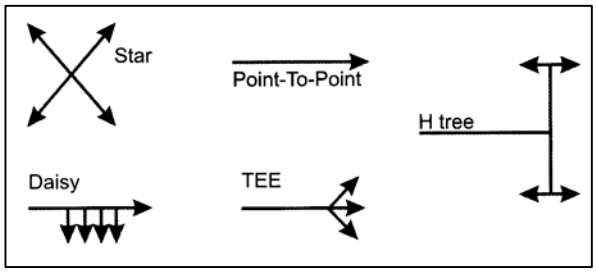

Figure 7: Various net topologies

The star topology is characterised by multiple branches from a central driving point that requires a strong driver. In this topology, series termination can be used, on each leg. However, if branch length matching is not possible, then RC termination close to central point can be used. In the case of the daisychain topology where loads are distributed down the line, together with a strong driver there will be skew between loads. As such, parallel, Thevenin or RC termination can be used. In point-to-point, connection between two points, when termination is required, a series resistor at the source is recommended, with a resistor value optimised for a rising or failing edge. This is dependent on how balanced the high/low impedance of the driver. In the case of TEE (Far end cluster), essentially a variation of star topology, where loads are close together and skew must be minimised. In this topology it is possible to use either series termination close to the driver, or RC termination at the branching point to the loads. Finally, the H tree topology is easier to drive than a star topology. With this method, each line from a tap to a load has the same impedance, so the same termination resistor value can be used at each load. The other advantage of the H-tree structure is that the wire length between the driver and each load is identical, preventing such signal skew problems.

8 GROUND BOUNCE

Outputs are inductively coupled between power and ground, as the component switches state. The sudden high current requirement will lead to a reverse voltage drop called ground bounce or switching noise. To minimise the effect, decoupling capacitors should be used (with low lead self inductance) and placed close to the component to be decoupled. The capacitor maintains a constant voltage across the component and delivers a more stable current outside of the general power planes. Since ground is more sensitive than VCC, the decoupling capacitor should be located as close as possible to the ground pin. Extra capacitance is provided by the use of multilayer PCB power and ground planes. In fact, ground bounce was the main contributing effect to the change from double sided to multilayer PCB with power and ground planes. Care should be taken when planes are getting heavily perforated, because this will cause the plane inductance to increase. Currents in an imperfect ground plane flow from ground pins to the power connector and can affect the voltage of other components with ground pins. High ground currents in the plane are more likely to occur with bus and high current drivers, they should therefore be located close to the power connector. It is important to ensure that self-resonant frequency of decoupling capacitors is above the frequency of the signal to be decoupled.

9 CROSSTALK

A high speed trace behaves like a transmitting antenna. A sudden change of current on one trace can cause capacitive and inductive coupling into adjacent traces. When this crosstalk level is sufficient, a false signal transition can occur. The amount of coupling between traces is proportional to the length of the two traces running in parallel and inversely proportional to their spacing. Strategies for the reduction of crosstalk include: minimising the length of parallelism; maximising trace spreading; lowering the thickness of the dielectric; minimising impedance; minimising the edge rate and selecting the most appropriate termination strategy.

10 CONCLUSIONS EMI REDUCTION TECHNIQUES

In order to reduce electromagnetic interference, there are a number of approaches including: minimising rise and fall times on clock and signal edges (see figure 8); utilising slowest logic consistent with the circuit operation (see figure 9); and board partitioning to minimise ground bounce effects (see figure 10).

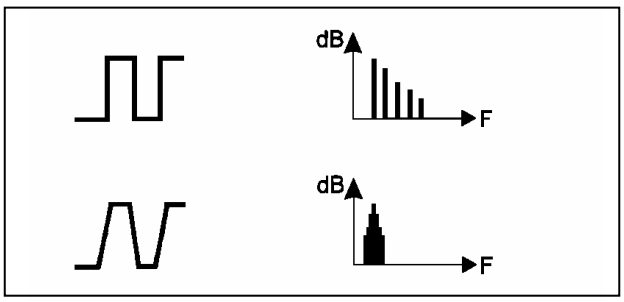

Figure 8: Minimising rise and small times on signal and clock edges

Minimised rise and fall times on signal and clock edges. Sharper edges cause high harmonic contents in the high frequency spectrum.

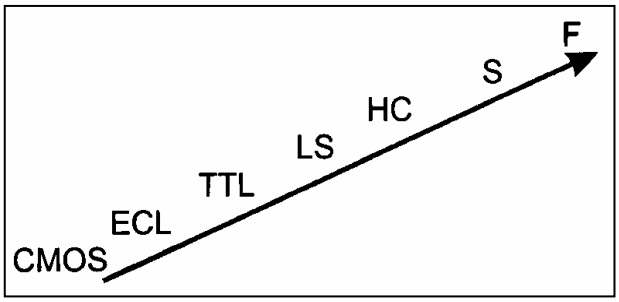

Figure 9: Using Slowest logic consistent with the circuit operation

Selection of the most appropriate logic family plays a key role in the overall EMC performance. Logic families that are designed to operate at high frequency will exhibit sharp edge rates. This will result in larger harmonic spectral contents. Figure 9 is ordered by the noisiest at the top to the less noisy at the bottom. The ECL family is relatively less noisy, this is simply because it has the small voltage swing. CMOS is slow and also has reduced drive capability, this is why it is the best from an EMC standpoint.

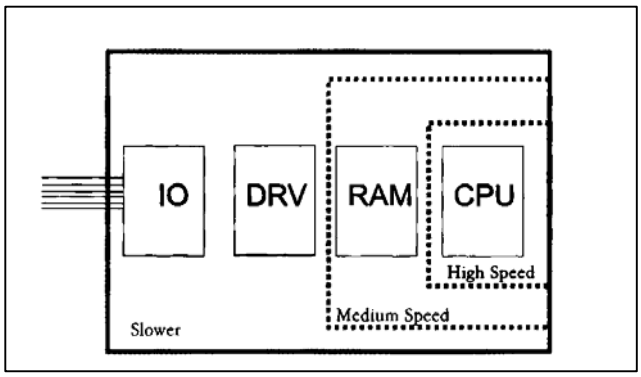

Figure 10: Board partitioning

To minimise ground bounce effect, it is desirable to place high speed components close to the power source with slower components placed further away. To minimise cross coupling and thus system noise it is also advisable to create separate partitions for analogue and digital sections. Furthermore, to prevent noise conducted through input/output IO cables, segregate IO connectors, IO drivers/receivers and non-IO components. Provide extra spacing between highly radiating nets and IO nets.

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